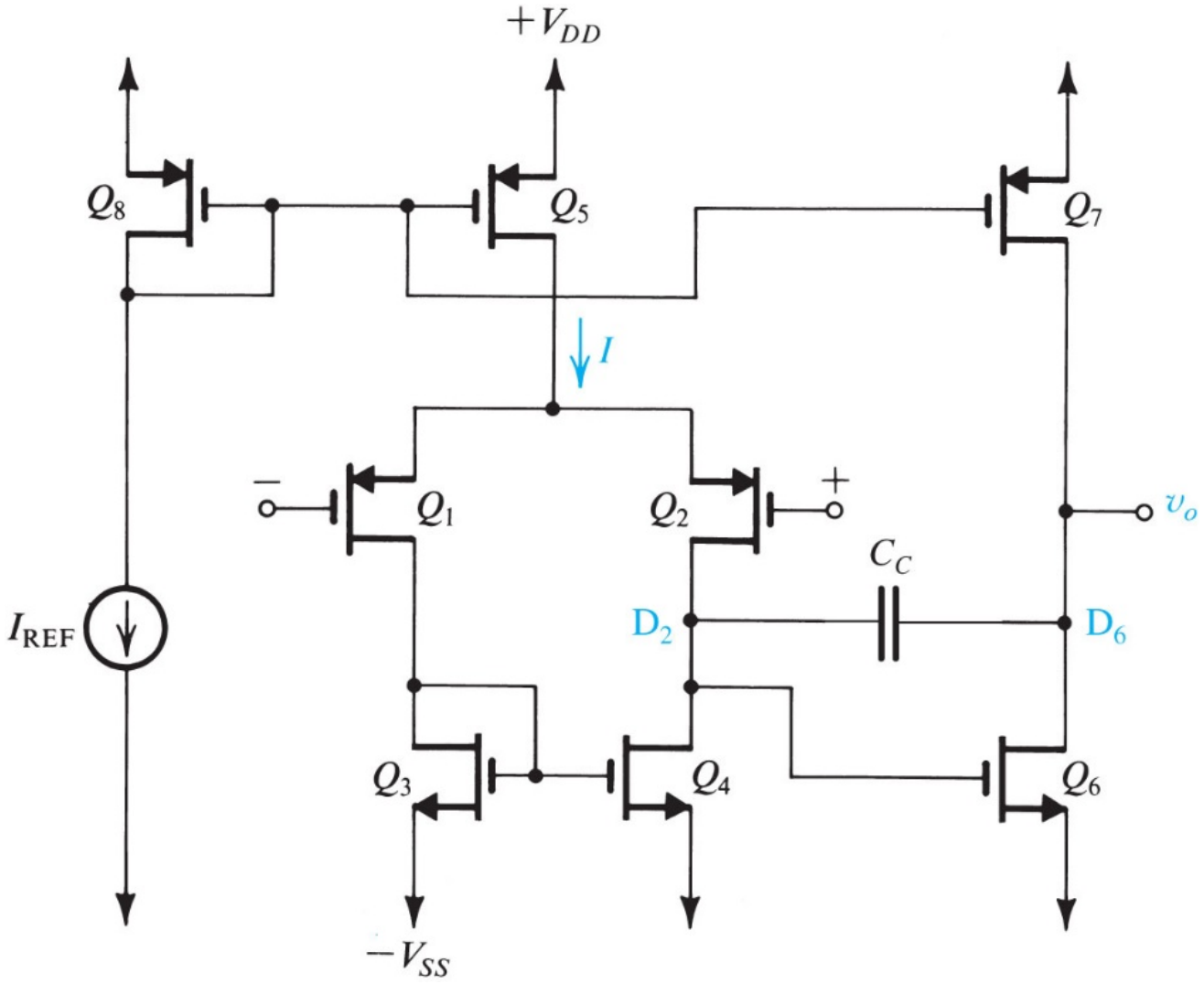
EE105
Microelectronic Devices and Circuits
Module 4-5: Differential Amplifiers

Prof. Ming C. Wu

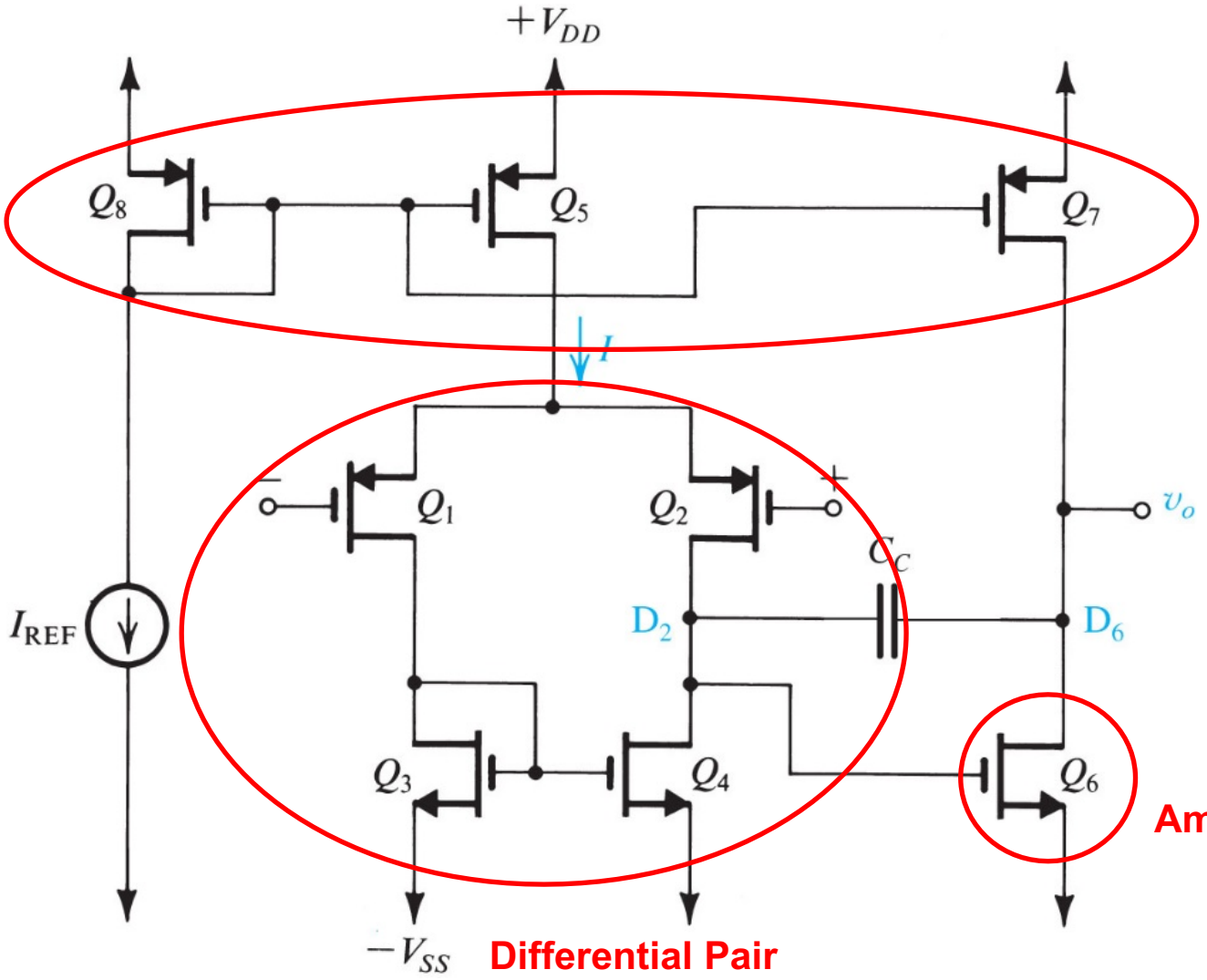
wu@eecs.berkeley.edu

511 Sutardja Dai Hall (SDH)

Two-Stage CMOS Op-Amp Circuit



Two-Stage CMOS Op-Amp Circuit

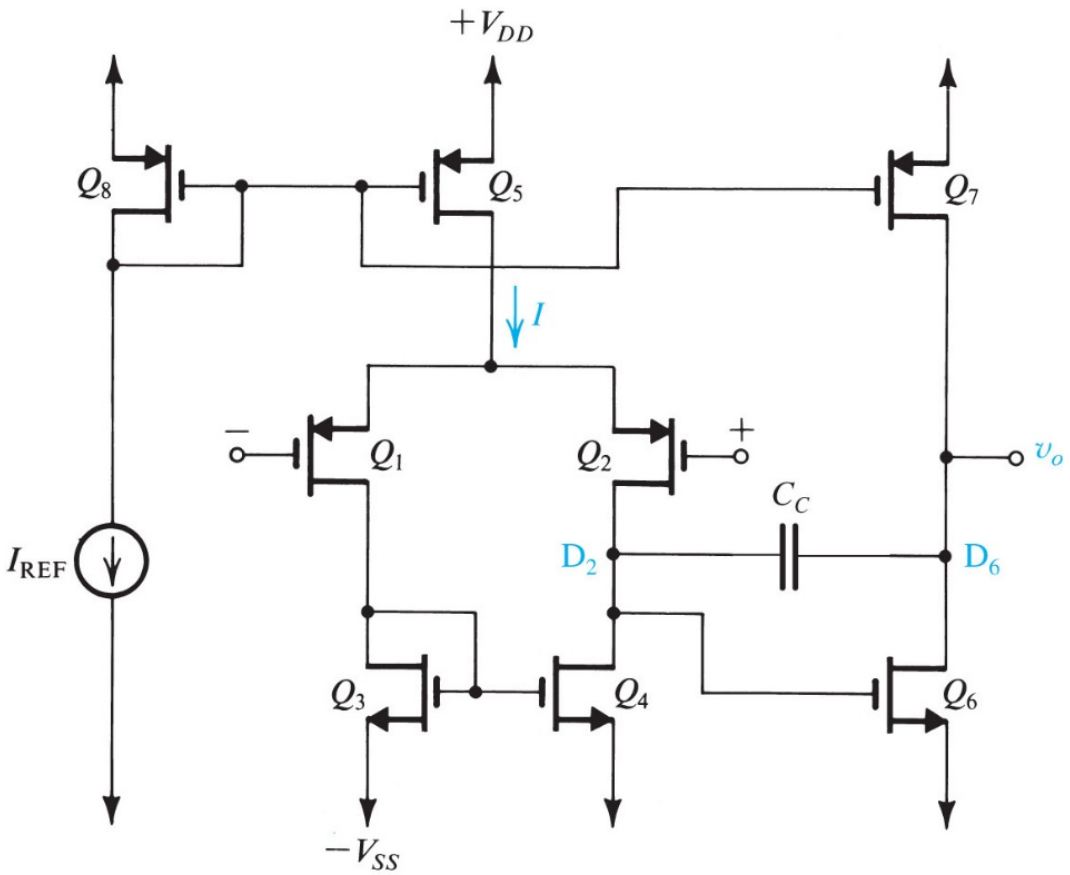


Current Mirrors

Common Source Amplifier Stage

Differential Pair with Current Mirror Load

Two-Stage CMOS Op-Amp Circuit



Voltage gain of the first stage (Q_1, Q_2): Differential input, single-ended output:

$$A_1 = -g_{m1}\left(r_{o2} \parallel r_{o4}\right)$$

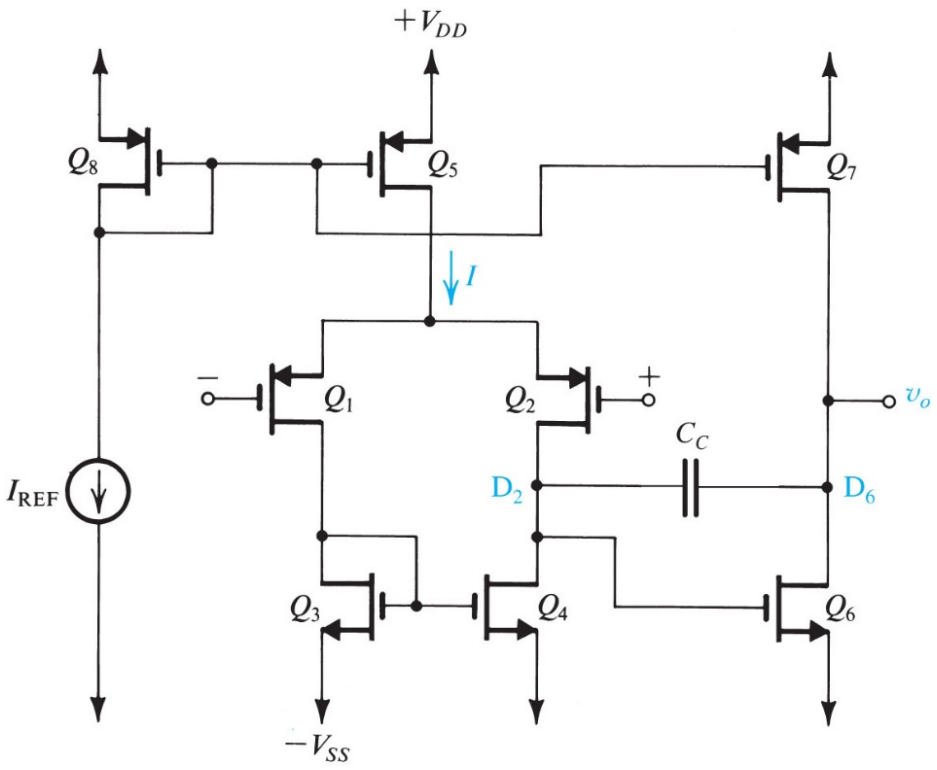
Voltage gain of the 2nd stage (Q_6): Common source with current source load:

$$A_2 = -g_{m6}\left(r_{o6} \parallel r_{o7}\right)$$

Total gain

$$A_o = A_1 A_2$$

Example:



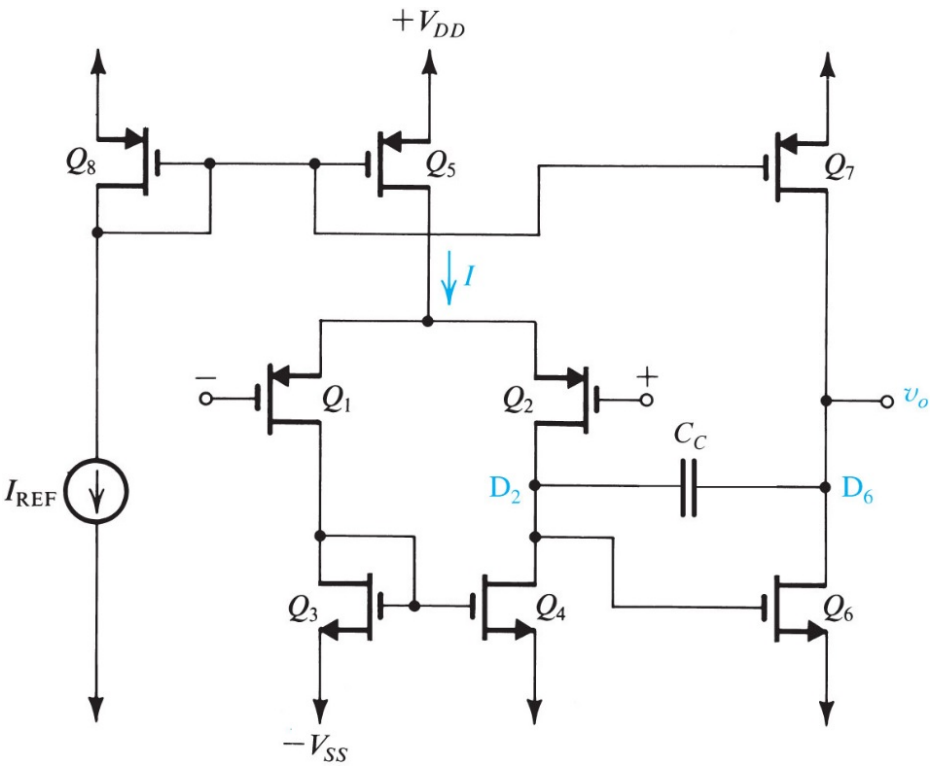
	Q1	Q2	Q3	Q4
W/L in um	20/0.8	20/0.8	5/0.8	5/0.8

	Q5	Q6	Q7	Q8
W/L in um	4/0.8	10/0.8	4/0.8	4/0.8

I_{REF} = 90 µA, V_{tn} = 0.7V, V_{tp} = -0.8V
$\mu_n C_{ox}$ = 160 µA/V², $\mu_p C_{ox}$ = 40 µA/V²
$|V_A|$ = 10V for all devices
$V_{DD} = V_{SS}$ = 2.5V

Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o for all Q's,
voltage gain,
input common mode range,
output voltage range.

Solution: DC Parameters



$$I_{REF} = 90\mu A$$

$$I_{D5} = \frac{(W/L)_5}{(W/L)_8} = 90\mu A$$

$$I_{D7} = \frac{(W/L)_7}{(W/L)_8} = 90\mu A$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2} = 45\mu A$$

$$I_{Di} = \frac{1}{2}\mu_i C_{ox}\left(\frac{W}{L}\right)|V_{OV}|^2$$

$$|V_{OV1}| = |V_{OV2}| = |V_{OV3}| = |V_{OV4}| = 0.3$$

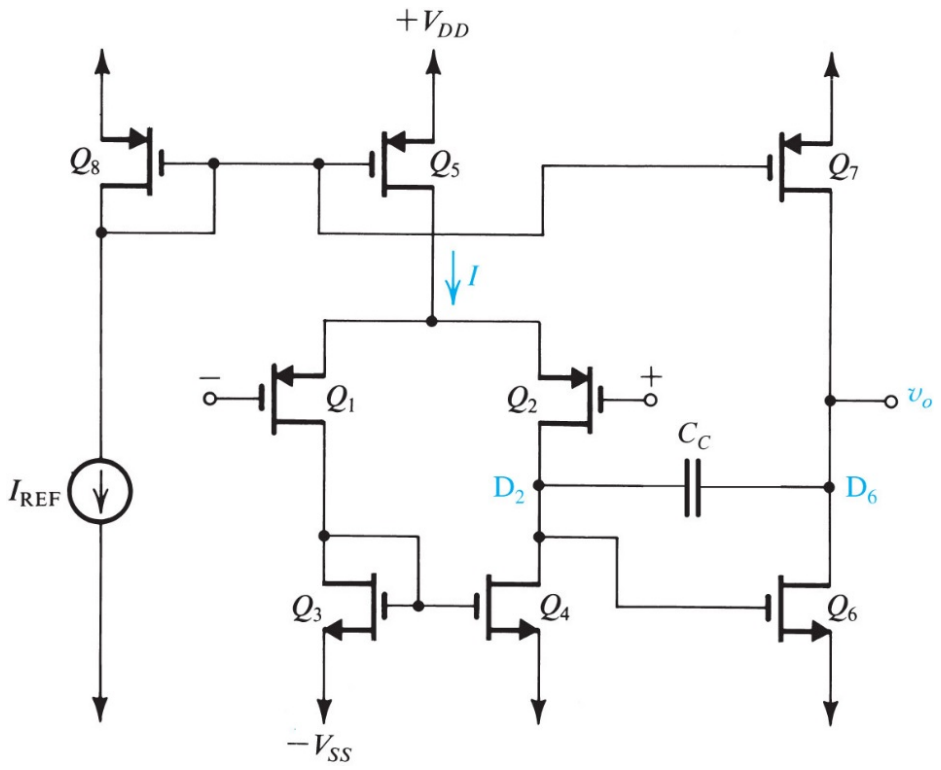
$$|V_{OV5}| = |V_{OV6}| = |V_{OV7}| = |V_{OV8}| = 0.3$$

$$|V_{GS}| = |V_{OV}| + |V_t|$$

$$\text{NMOS}: |V_{GS}| = 0.3 + 0.7 = 1.0V$$

$$\text{PMOS}: |V_{GS}| = 0.3 + 0.8 = 1.1V$$

Solution: AC Parameters



$$g_m = \frac{2I_D}{|V_{OV}|}$$

$$g_{m1-4} = 2 \times 45\mu A / 0.3V = 0.3mA / V$$

$$g_{m5-8} = 2 \times 90\mu A / 0.3V = 0.6mA / V$$

$$r_o = \frac{|V_A|}{I_D}$$

$$r_{o1-4} = \frac{10V}{45\mu A} = 222k\Omega$$

$$r_{o5-8} = \frac{10V}{90\mu A} = 111k\Omega$$

$$A_1 = -g_{m1}\left(r_{o2} \parallel r_{o4}\right)$$

$$= -0.3 \times 222 / 2 = -33.3V / V$$

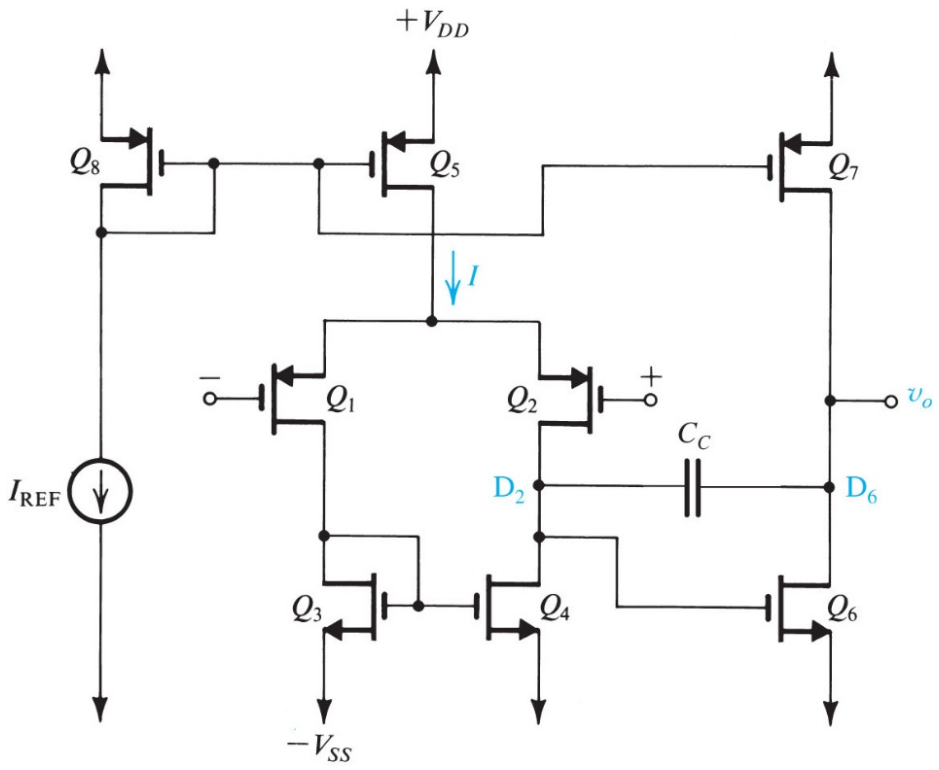
$$A_2 = -g_{m6}\left(r_{o6} \parallel r_{o7}\right)$$

$$= -0.6 \times 111 / 2 = -33.3V / V$$

$$A_o = A_1 A_2 = 1109V / V$$

$$= 20\log(1109) = 61dB$$

Solution: Input Common-Mode Ranges



Input common-mode voltage range:

Maximum: Q_5 near edge of saturation

$$|V_{DS5}| = |V_{OV5}| = 0.3V$$

$$v_{icm\max} = 2.5 - |V_{OV5}| - |V_{GS5}|$$

$$= 2.5 - 0.3 - 1.1 = 1.1V$$

Minimum: Q_1 near edge of saturation

$$v_{D1} = -V_{SS} + V_{GS3} = -2.5 + 1 = -1.5V$$

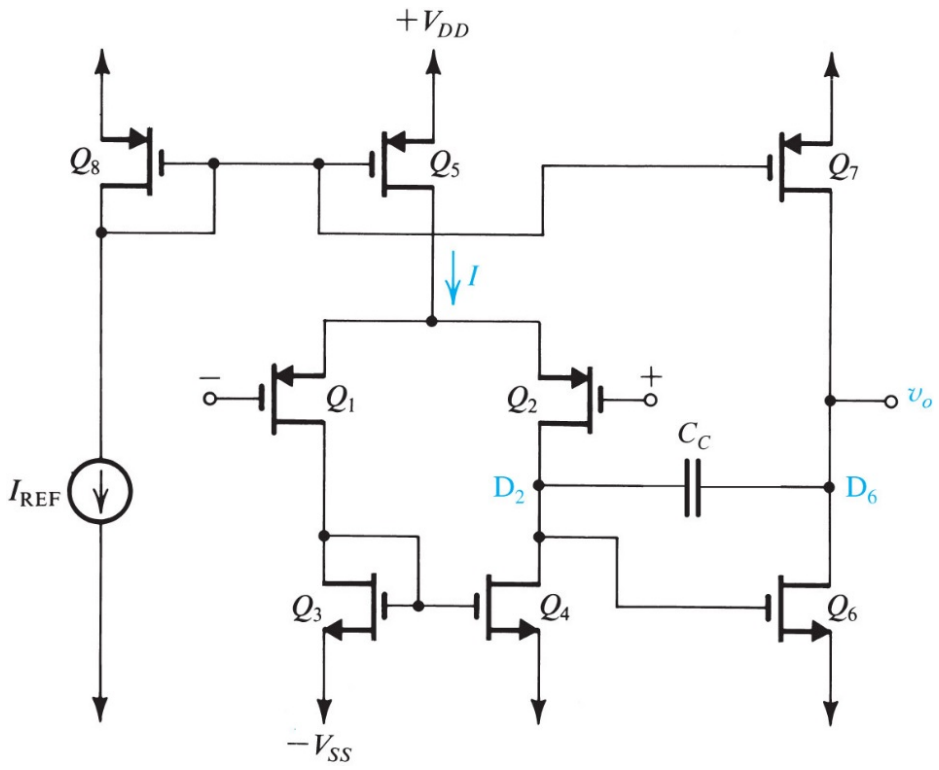
$$|v_{DS1}| = |v_{GS1}| - |v_{tp}|$$

$$-v_{DS1} = -v_{GS1} - 0.8$$

$$-v_{D1} = -v_{G1} - 0.8$$

$$v_{icm\min} = v_{G1} = v_{D1} - 0.8 = -2.3V$$

Solution: Output Ranges



Output voltage range:

Maximum: Q_7 near edge of saturation

$$|V_{OV7}| = 0.3V$$

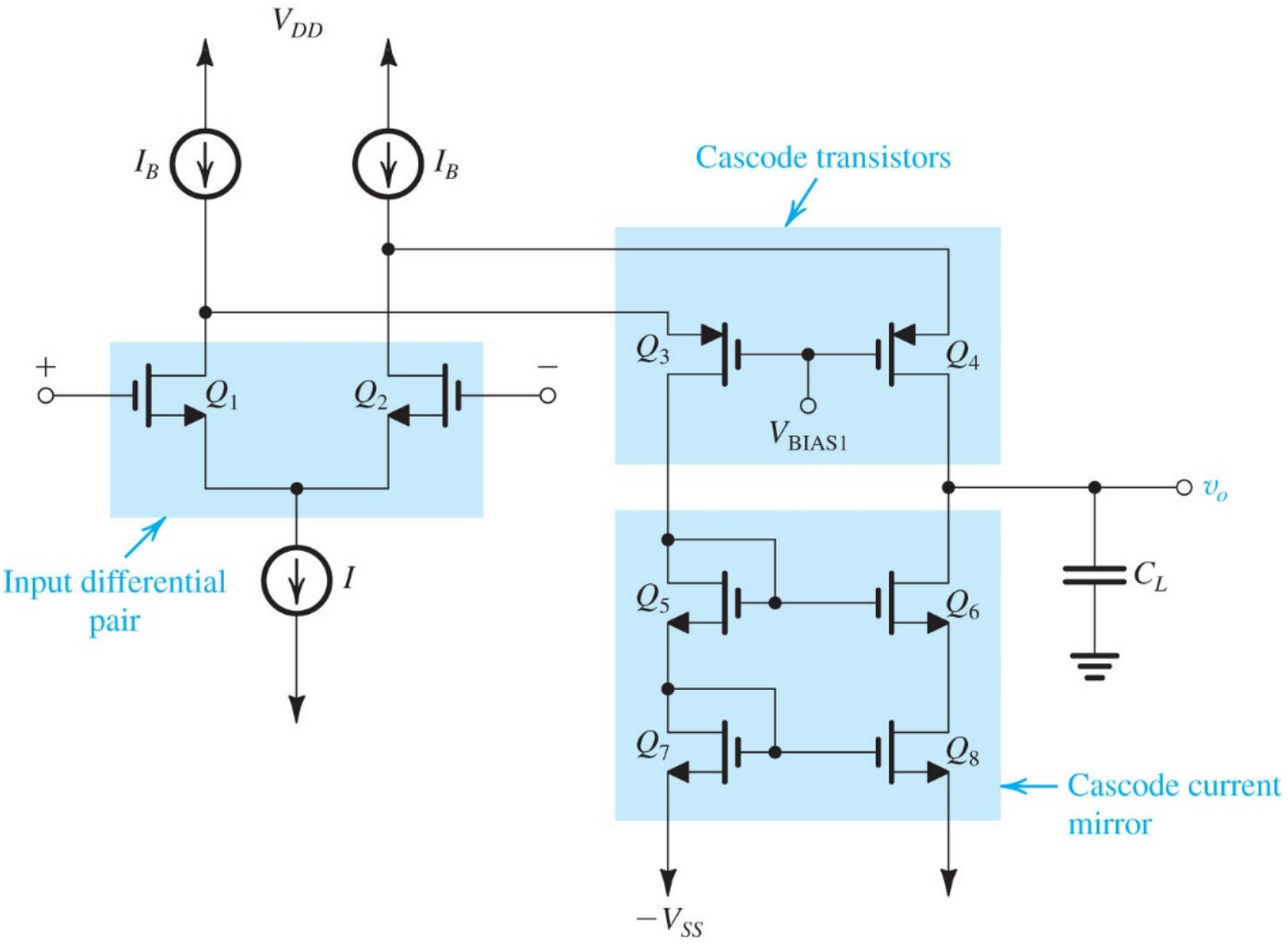
$$v_{o\max} = 2.5 - |V_{OV7}| = 2.2V$$

Minimum: Q_6 near edge of saturation

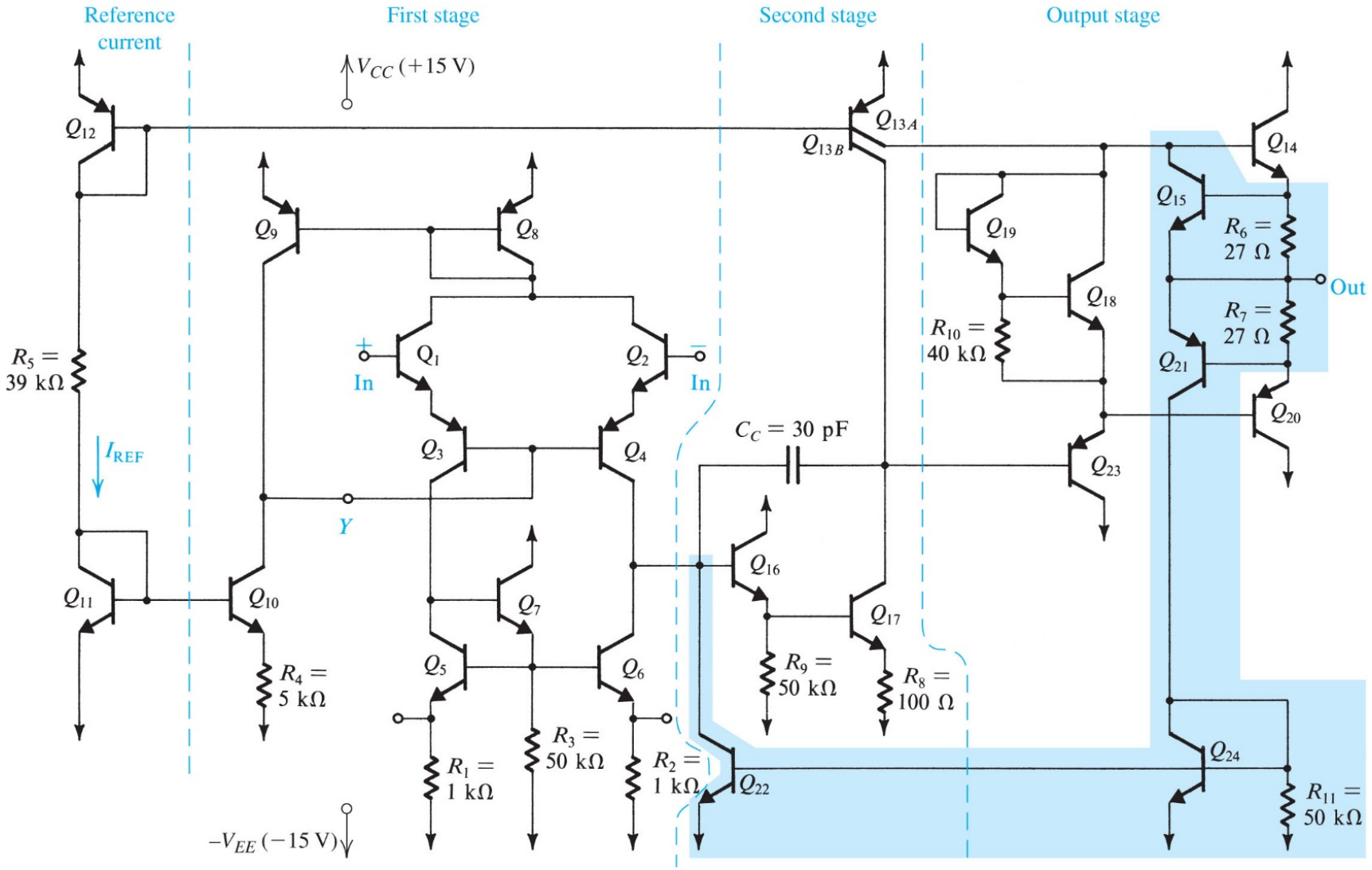
$$v_{o\min} = -V_{SS} + |V_{OV6}| = -2.5 + 0.3 = -2.2V$$

Folded-Cascode CMOS Op Amp.

(for inspection only)



741 Op-Amp Circuit



Functions of Various Transistors

- Q_{11}, Q_{12}, and R_5 generate a reference bias current, I_{REF}.
- Q_{10}, Q_9, and Q_8 bias the input stage, which is composed of Q_1 to Q_7.
- The second gain stage is composed of Q_{16} and Q_{17} with Q_{13B} acting as active load.
- The class AB output stage is formed by Q_{14} and Q_{20} with biasing devices Q_{13A}, Q_{18}, and Q_{19}, and an input buffer Q_{23}.
- Transistors Q_{15}, Q_{21}, Q_{24}, and Q_{22} serve to protect the amplifier against output short circuits and are normally cut off.